ALPHA DATA

ADM-VPX3-7V2
User Manual

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1 Introduction

The ADM-VPX3-7V2 is a high-performance XMC for applications using Virtex-7 FPGAs from Xilinx. This card supports Virtex-7 devices available in the FF(G), FH(G), and FL(G), 1761 package.

The ADM-VPX3-7V2 includes a separate FPGA with a PCIe bridge developed by Alpha Data. Using a separate device allows high performance operation without the need to integrate proprietary cores in the user (target) FPGA.

With the release of 7series FPGA boards, Alpha Data has introduced a new build option to allow the mezzanine card to be assembled without the bridge to reduce power and cost.

The ADM-VPX3-7V2 is available in air-cooled and conduction-cooled configurations (with 2 Level Maintenance compatibility). View the ADM-VPX3-7V2 Ordering Info tab at ADM-VPX3-7V2 Product Page on www.alpha-data.com.

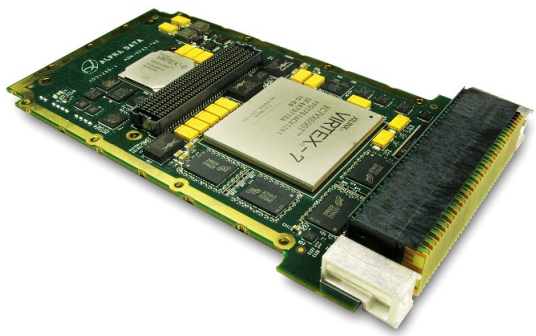

Figure 1 : ADM-VPX3-7V2 Product Picture

1.1 Key Features

Key Features
Open VPX Compliance List

- 3U Open VPX, compliant to VITA Standard 46.0 and 65
- Dedicated 4-lane PCI-Express Gen 2 interface with high-performance DMA controllers
- 4 additional PCI-Express compliant GTX links between user FPGA and OpenVPX Data Plane
- 4 lane Expansion port compliant to OpenVPX
- 2 Control plane connections, one to user FPGA, one to Bridge
- P2 Connector compliant to Vita 46.9 X24S+X8D+X12D
- Support for Virtex-7 FPGA in FF(G), FH(G), and FLG(G)1761 package
- 4 independent banks of DDR3-1600 SDRAM, 512MB/bank, 2GB total (4GB option)
- FMC front panel interface compliant with Vita 57.1 utilizing all IO and all High-Speed links.
- 1PPS Capable via OpenVPX AUXCLK
- Clock synchronization with OpenVPX REFCLK
- On-board programmable clocks enabling multiple protocols to be implemented on the user FPGA's high-speed links
- Voltage and temperature monitoring
- Air-cooled, conduction-cooled, and 2 Level Maintenance configurations available
- SLT3-PAY-2F1F2U-14.2.1

- SLT3-PAY-1F2F2U-14.2.2
- SLT3-PAY-2F2U-14.2.3
- SLT3-PAY-1F1F2U-14.2.4
- SLT3-PAY-1D-14.2.6
- SLT3-PAY-2F-14.2.7
- SLT3-PAY-1F4U-14.2.8
- SLT3-PAY-8U-14.2.9
- SLT3-PER-2F-14.3.1
- SLT3-PER-1F-14.3.2
- SLT3-PER-1U-14.3.3

1.2 References & Specifications

ANSI/VITA 46.0	VPX Baseline Standard, October 2007, VITA, ISBN 1-885731-44-2
ANSI/VITA 46.9	PMC/MXC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard, November 2010, VITA, ISBN 1-885731-63-9
ANSI/VITA 48.2	Mechanical Specifications for Microcomputers Using REDI Conduction Cooling Applied to VITA VPX, July 2010, VITA, ISBN 1-885731-60-4
ANSI/VITA 57.1	FPGA Mezzanine Card (FMC) Standard, February 2010, VITA, ISBN 1-885731-49-3
ANSI/VITA 65	OpenVPX™ System Specification, June 2010, VITA, ISBN 1-885731-58-2

Table 1 : References

2 Installation

2.1 Software Installation

Please refer to the Software Development Kit (SDK) installation CD. The SDK contains drivers, examples for host control and FPGA design with comprehensive help on application interfacing.

2.2 Hardware Installation

2.2.1 System Requirements

The ADM-VPX3-7V2 is a 3U OpenVPX compliant FPGA card with FMC front IO interface. To use the Alpha Data's powerful API and drivers, the system controller must be capable of driving the PCIe lanes to the Bridge. The ADM-VPX3-7V2 also utilizes the OpenVPX 1000Base-X control lines, though this implementation is left to the user.

P2 complies with Vita 46.9 X24S+X8D+X12D user defined pin configuration with an additional 8 connections to P2 Row G. The X24s can be configured as either 24 songle ended signals at 3.3V or 12 LVDS pairs (but not both). The eight user defined single ended connections in row G are 3.3V compliant and can be isolated from the backplane via onboard switches.

Alpha Data offers a Rear Transition Module (RTM) that breaks out all P2 IO and P1 control lanes for use in lab and development environments (Part number: ADM-VPX3-7V2-RTM).

The ADM-VPX3-7V2 can be configured to either utilize 5V or 12V as the main power source. The default build uses 5V, contact sales@alpha-data.com for details on the 12V build option.

2.2.2 Cooling Requirements

The power dissipation of the board is highly dependent on the Target FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the approximate current requirements for each power rail.

The board is supplied with a passive air cooled or conduction cooled heatsink according to the order number given at time of purchase. It is the users responsibility to ensure sufficient airflow for air cooled applications and appropriate metalwork for conduction cooled applications.

The board features system monitoring that measures the board and FPGA temperature. It also includes a self-protection mechanism that will clear the target FPGA configuration if an over-temperature condition is detected.

See Section Health Monitoring for health monitoring details.

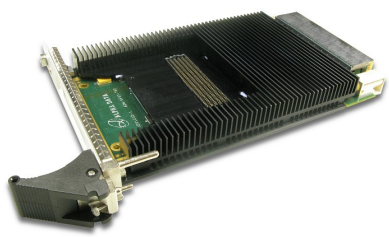

Figure 2 : ADM-VPX3-7V2 Air Cooled

3 Functional Description

3.1 Overview

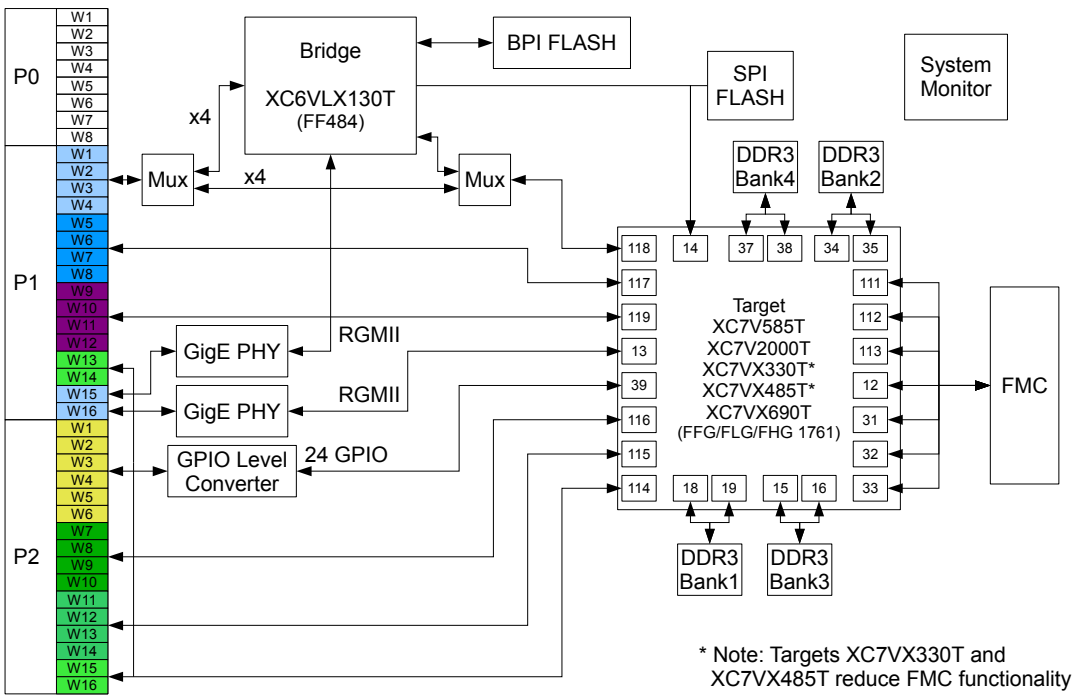

Figure 3 : ADM-VPX3-7V2 Block Diagram

3.1.1 Switch Definitions

There is a set of eight DIP switches placed on the bottom of the board. Their functions are described in Table Switch Definitions.

Note:
All switches are OFF by default. Factory Configuration switch must be in the OFF position for normal operation.

Switch Ref.	Function	ON State	Off State
SW1-1	P2 LVDS	24s on P2 use CMOS	24s on P2 use LVDS
SW1-2	Internal Oscillator	Use VPX REFCLK	Use Internal Oscillator source
SW1-3	Bridge Bypass	Bridge FPGA is bypassed - PCIe lanes (3:0) are connected directly to the user FPGA.	Bridge FPGA is used. PCIe lanes (3:0) are connected to the bridge.
SW1-4	Flash Boot Inhibit	Target FPGA is not configured from onboard flash memory.	Target FPGA is configured from on-board flash memory.
SW1-5	VPX JTAG	Connect JTAG chain to P0	Isolate JTAG chain from P0
SW1-6	E-Fuse	Enable E-Fuse programming voltage (VccEFuse = 2.5V)	Disable E-Fuse programming voltage (VccEFuse = 0V)
SW1-7	Factory Configuration	-	Normal Operation
SW1-8	Bridge-Less Mode	Bridge-Less Mode Active - User bitstream loaded from SPI flash	PCIe Bridge Mode Active - User bitstream loaded from Bridge

Table 2 : Switch Definitions

3.1.2 LED Definitions

The position and description of the board status LEDs are shown in Figure LED Locations:

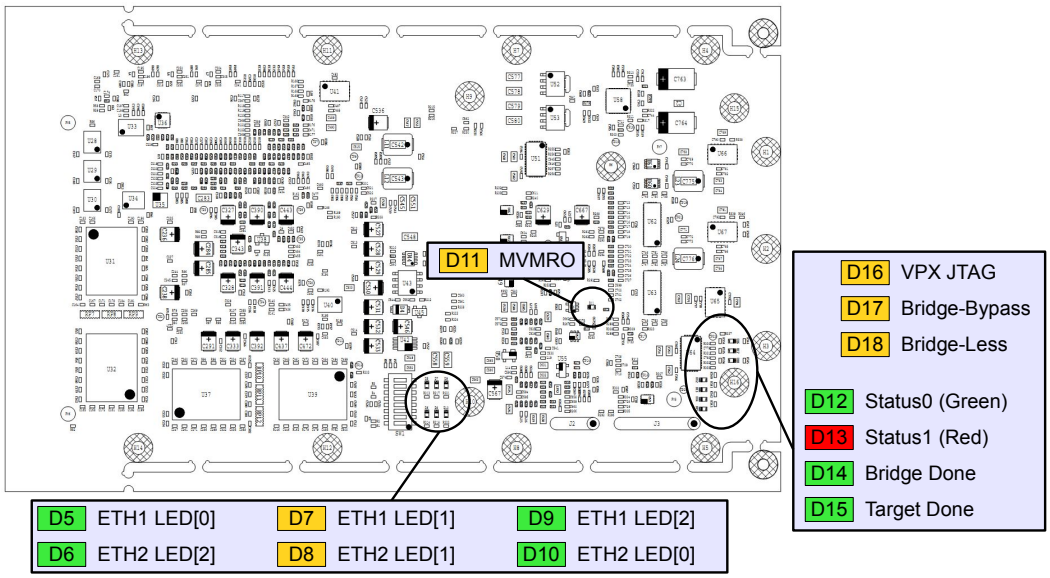

Figure 4 : LED Locations

Comp. Ref.	Function	ON State	Off State
D11(Amber)	MVMRO	Inhibit writes to non-volatile memories	Enable writes to non-volatile memories
D12(Green)	Status 0	See section Microcontroller Status LEDs	ERROR
D13(Red)	Status 1	See section Microcontroller Status LEDs	ERROR
D14(Green)	Bridge Done	Bridge FPGA is configured	Bridge FPGA is unconfigured
D15(Green)	Target Done	Target FPGA is configured	Target FPGA is unconfigured
D16(Amber)	XMC JTAG	JTAG chain connected to P0	JTAG chain is isolated from P0
D17(Amber)	Bridge Bypass	Bridge FPGA is bypassed - PCIe lanes (3:0) direct to user FPGA	Bridge FPGA is used. PCIe lanes (3:0) are connected to the bridge.
D18(Amber)	Bridge-Less	Target is configured by SPI memory	Target is configured by Bridge
D5(Green)	ETH1 LED[0]	Link	No Link
D6(Green)	ETH2 LED[2]	Link	No Link
D7(Amber)	ETH1 LED[1]	Receive	No Receive
D8(Amber)	ETH2 LED[1]	Receive	No Receive
D9(Green)	ETH1 LED[2]	Link	No Link
D10(Green)	ETH2 LED[0]	Link	No Link

Table 3 : LED Definitions

3.2 VPX P0 Interface

3.2.1 MVMRO

Non-Volatile Memory Read Only. This signal is an input from the system. When asserted (high), all writes to non-volatile memories are inhibited. This is indicated by the Amber LED, D7.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the target FPGA.

3.2.2 SYSRESET#

XMC Reset In. This signal is an active low input from the system. When asserted, the bridge FPGA will be reset. This also acts and PCI Reset.

The SYSRESET# signal is translated to 1.8V levels and connected to the target FPGA at pin AF30.

3.2.3 AUXCLK

Auxiliary Clock. This clock is a direct input to the target FPGA. In OpenVPX this clock line is used for 1PPS synchronization signaling. AUXCLK is limited to 1.8V by a quickswitch and the prefered signaling standard is LVDS.

AUXCLK_P is connected to Target FPGA MRCC pin G14

AUXCLK_N is connected to Target FPGA MRCC pin G13

3.2.4 REFCLK

Reference Clock. This clock is an input to the onboard clock distribution and generation system. The 50MHz defined in OpenVPX can be used to align all system clocks. Alternatively an onboard 50MHz reference can be generated as shown in Table Switch Definitions.

3.3 VPX P2 GPIO

3.3.1 LVDS

When SW1-1 is OFF, the GPIO on P2 is compatible with 1.8V signaling such as LVDS and 1.8V single ended signals.

These signals are routed differentially as shown in the pinout tables in the appendix. The FPGA is protected from inappropriate signal levels by an NXP 74CBTLVD3861 which is a low resistance quick switch that clamps at 1.8V in either direction, but can accept up to 3.3V on an input.

3.3.2 CMOS

When SW1-1 is ON, the GPIO on P2 is compatible with 3.3V signaling such as TTL and CMOS.

The signals are passed through a TI TXS0108ERGYR open-drain, push-pull, compatible auto direction sensing level translator. This protects the FPGA from higher voltages on the backplane while allowing it to communicate at 3.3V levels, compliant with CMOS and TTL voltages. The level translator has a propagation delay of 5.7ns max and a channel-to-channel skew (within a package) of 1ns. Therefore, it is only suitable for rates up to ~50Mb/s

3.4 JTAG Interface

3.4.1 On-board Interface

A JTAG boundary scan chain is connected to header J3. This allows the connection of the Xilinx JTAG cable for FPGA debug using the Xilinx ChipScope tools.

The JTAG Header pinout is shown in Figure JTAG Header J3:

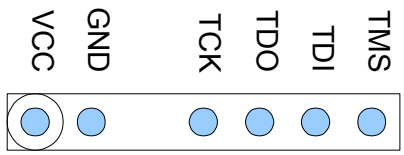

Figure 5 : JTAG Header J3

The scan chain is shown in Figure JTAG Boundary Scan Chain:

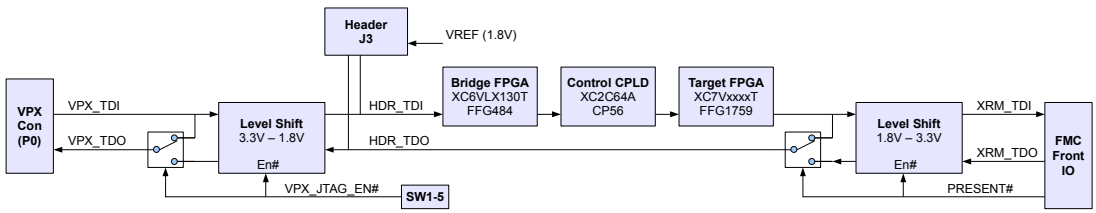

Figure 6 : JTAG Boundary Scan Chain

If the boundary scan chain is connected to the interface at the VPX backplane (SW1-5 is ON), header J3 should not be used.

3.4.2 VPX Interface

The JTAG interface on the VPX backplane is normally unused. When SW1-5 is OFF (default), all JTAG signals to P0 are left floating.

The JTAG interface can be connected to the VPX Backplane (through level-translators) by switching SW1-5 ON. See Table Switch Definitions

3.4.3 JTAG Voltages

The on-board JTAG scan chain uses 1.8V. The Vcc supply provided on J3 to the JTAG cable is +1.8V and is protected by a poly fuse rated at 350mA. 3.3V signals must not be used at header J3.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

The JTAG signals at the FMC interface use the 3.3V and are level shifted up from 1.8V in the rest of the card.

3.5 Clocks

The ADM-VPX3-7V2 provides a wide variety of clocking options. Fixed clocks at 200MHz and 250MHz are distributed throughout the FPGA. Additionally, the ADM-VPX3-7V2 provides 4 user-programmable clocks. These clocks can be combined with the FPGA's internal PLLs to suit a wide variety of communication protocols.

A complete overview of the clock routing on the ADM-VPX3-7V2 is given in Figure Clocks. A description of each clock follows.

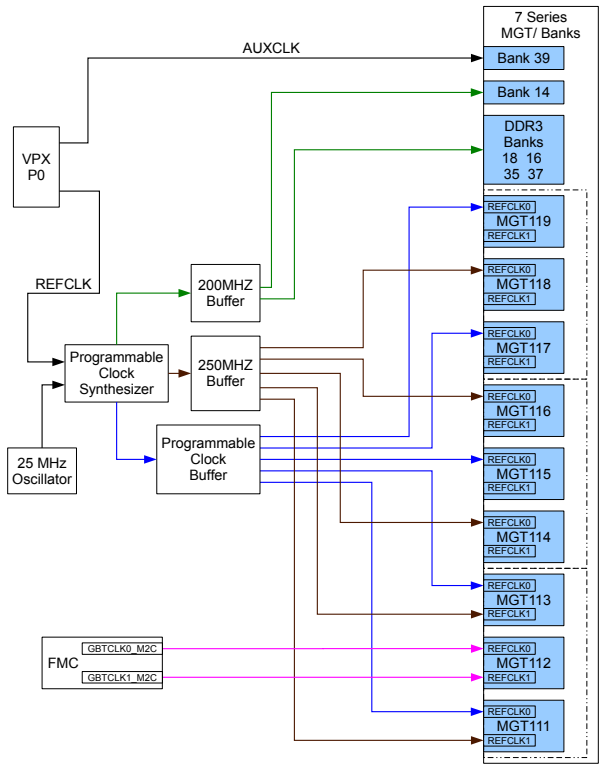

Figure 7 : Clocks

Note:
Clock Termination
The LVDS clocks do not have termination resistors on the circuit board. On-die terminations in the FPGA must be enabled by setting the attribute "DIFF_TERM = TRUE". This can either be set in the source code when instantiating the buffer, or in the User Constraints File (UCF). See the Xilinx Virtex-7 Libraries Guide and Constraints Guide for further details.

Note:
Super Logic Region (SLR)
While most MGT clocks can be shared to the tile north and south of the receiving tile, 2000T devices employ stacked silicon interconnect technology and are limited by SLRs. MGT clocks can only be shared within a SLR to the tile north or south of their receiving tile. SLRs are shown by dotted lines in Figure Clocks.

3.5.1 200MHz Reference Clock (REFCLK200M)

The fixed 200MHz reference clock REFCLK200M is a differential clock signal using LVDS.

REFCLK200M is connected to a MRCC inputs on the Target FPGA on Bank 14.

REFCLK200M is also converted to HSTL signaling and used as the input clock for the DRAM interface.

This clock can be used to generate application-specific clock frequencies using the PLLs within the Virtex-7 FPGA. It is also suitable as the reference clock for the IO delay control block (IDELAYCTRL).

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK200M	200 MHz	IO_L12_T2_MRCC_14	LVDS	AK34	AL34
REFCLK200M_HSTL	200 MHz	IO_L13_T1_MRCC_16	HSTL_I	AD32	AD33
REFCLK200M_HSTL	200 MHz	IO_L13_T1_MRCC_18	HSTL_I	U36	T37
REFCLK200M_HSTL	200 MHz	IO_L13_T1_MRCC_35	HSTL_I	E34	E35
REFCLK200M_HSTL	200 MHz	IO_L13_T1_MRCC_37	HSTL_I	D27	D28

Table 4 : REFCLK200M Connections

3.5.2 250MHz Reference Clock (REFCLK200M)

The fixed 250MHz reference clock REFCLK250M is a differential clock signal using LVDS.

REFCLK250M is connected to MGT REFCLK inputs on the Target FPGA.

This clock is ideal for PCIe reference clocking and many other communication standards.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK250M	250 MHz	MGTREFCLK0_118	LVDS	E10	E9
REFCLK250M	250 MHz	MGTREFCLK0_116	LVDS	T8	T7
REFCLK250M	250 MHz	MGTREFCLK0_114	LVDS	AD8	AD7
REFCLK250M	250 MHz	MGTREFCLK1_113	LVDS	AK8	AK7
REFCLK250M	250 MHz	MGTREFCLK1_111	LVDS	BA10	BA9

Table 5 : REFCLK250M Connections

3.5.3 Programmable Clocks (LCLK, PROGCLK 0-4)

There are two programmable clock sources that are forwarded throughout the FPGA. These clocks are programmable through the Alpha Data ADM-XRC Gen 3 SDK. LCLK is generated in the Bridge FPGA by the Alpha Data ADB3 driver and offers a less accurate frequency resolution, but with a wider programmable frequency range. PROGCLK[4:0] is generated by a dedicated programmable clock generator IC and offers extremely high frequency resolutions (1ppm increments). PROGCLK[4:0] is generated by a single source and buffered to all MGT tiles at the same frequency and phase.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
LCLK	5 - 700 MHz	IO_L13_MRCC_14	LVDS	AJ32	AK32
PROGCLK0	5 - 312.5 MHz	MGTREFCLK0_119	LVDS	A10	A9
PROGCLK1	5 - 312.5 MHz	MGTREFCLK0_117	LVDS	K8	K7
PROGCLK2	5 - 312.5 MHz	MGTREFCLK0_115	LVDS	Y8	Y7
PROGCLK3	5 - 312.5 MHz	MGTREFCLK0_113	LVDS	AH8	AH7
PROGCLK4	5 - 312.5 MHz	MGTREFCLK0_111	LVDS	AW10	AW9

Table 6 : PROGCLK Connections

3.5.4 FMC-Carrier MGT Clock (MGTCLK_M2C)

The reference clocks "GBTCLK0_M2C" and "GBTCLK1_M2C" are differential clock signals using LVDS. The clock is provided by an FMC module through the FMC interface. It is connected at MGT 112 on the Target FPGA for application specific frequencies / line rates.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
GBTCLK0_M2C	Variable	MGTREFCLK0_112	LVDS	AT8	AT7
GBTCLK1_M2C	Variable	MGTREFCLK1_112	LVDS	AU10	AU9

Table 7 : MGTCLK_M2C Connections

3.5.5 FMC-Carrier Signal Clocks (GCLK_M2C)

The FMC interface utilizes numerous clock capable and clock dedicated connections between the FPGA and the FMC module. The ADM-VPX3-7V2 connects all possible clock pins on the FMC interface to clock capabel IO on the FPGA. Please see Appendix Clock Pins for more details.

3.5.6 25MHz Source

Early board revisions used a Fox oscillator, type FXO-LC526R-25.00, which has total stability = ±25ppm. Current models use the SiLabs 511FCA25M0000BA9, with has total stability = ±30ppm.

3.6 Flash Memory

A 512Mb Flash Memory (Intel / Numonyx PC28F512P30EF) is used to store configuration bitstreams for the Bridge and Target FPGAs.

The flash memory cannot be accessed by the target FPGA. Host access is only possible through the FLCTL, FLPAGE and FLDATA registers in the Bridge FPGA.

The region of memory between addresses 0x11000000 and 0x11FFFFF is allocated for custom data to be stored by the ADM-VPX3-7V2 user.

Utilities for erasing, programming and verification of the flash memory are provided in the ADMXRC SDK.

Write Protect

The Flash Write Protect (WP#) pin is connected to an inverted version of the NVMRO signal at the XMC interface. When the NVMRO signal is active (High), all writes to the flash will be inhibited. This state will be indicated by the Amber LED as shown in Figure LED Locations.

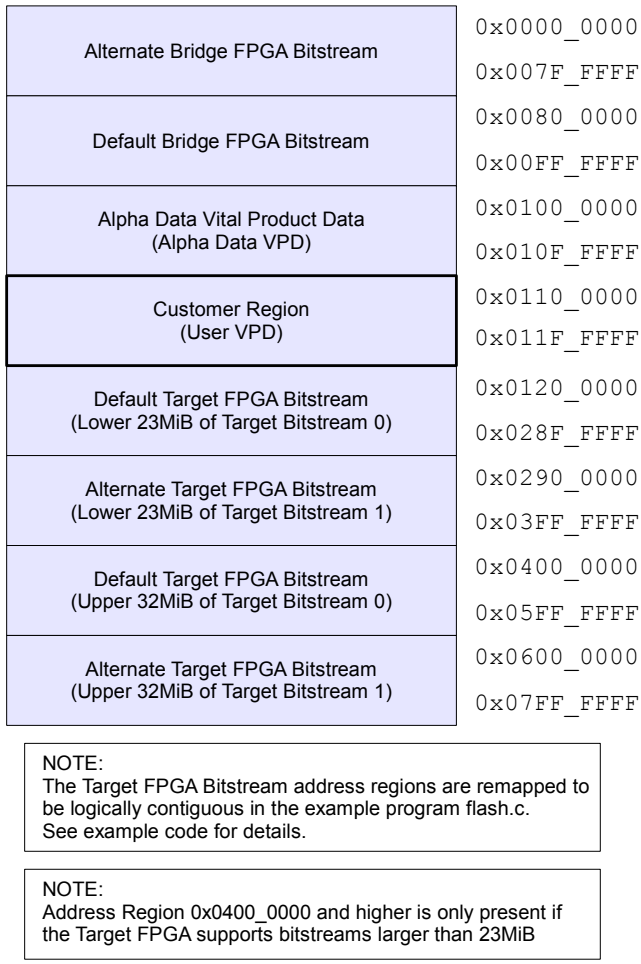

Figure 8 : Flash Memory Map

3.7 Configuration

3.7.1 Power-Up Sequence

If valid data is stored in the flash memory, the bridge will automatically configure the Target FPGA at power-up.

This sequence can be inhibited by turning the Flash Boot Inhibit (FBI) switch. (See Table Switch Definitions).

Note:
If an over-temperature alert is detected from the System Monitor, the target will be cleared by pulsing its PROG signal. See Section Automatic Temperature Monitoring.

3.7.2 Bridge-Less Mode

When operating in bridgeless mode, the Target FPGA will be configured directly by a Quad SPI connection to a 512Mb FLASH memory device. This memory device is re-programable over a Xilinx JTAG cable.

3.8 Health Monitoring

The ADM-VPX3-7V2 has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using the ATMEGA128 microcontroller.

Control algorithms within the microcontroller automatically check line voltages and on board temperatures and shares the information with blockram in the Bridge FPGA.

The following voltage rails and temperatures are monitored:

Monitor	Purpose
1.0V	FPGA Core Supply (VccINT)
1.0V	Target Transceiver Power (AVCC)
1.2V	Target Transceiver Power (AVTT)
1.2V	Bridge Transceiver Power (AVTT)
1.5V	DDR3 SDRAM, Target FPGA memory I/O
FMC_VADJ	(Front-Panel) I/O voltage (1.8V or lower)
1.8V	Target Transceiver Power (AVCC_AUX)
1.8V	Flash Memory, FPGA IO Voltage (VCCO)
2.0V	Target FPGA Auxiliary Supply AUX (VccAUX)
2.5V	Level Translation, Bridge FPGA Auxiliary Supply (VccAUX)
3.3V	From VPX P0
5.0V	From VPX P0
12.0V	From VPX P0
Temp1	Target FPGA on-die temperature
Temp2	Board temperature sensor on-die temperature
Temp3	Bridge FPGA on-die temperature

Table 8 : Voltage and Temperature Monitors

An example application that reads the system monitor ("sysmon") is available within the SDK.

3.8.1 Automatic Temperature Monitoring

At power-up, the control logic sets the temperature limits and resets the LM87's over-temperature interrupt.

The temperature limits are shown in Table Temperature Limits:

	Target FPGA		Bridge FPGA		Board	
	Min	Max	Min	Max	Min	Max
Commercial	0 degC	+85 degC	0 degC	+85 degC	0 degC	+85 degC
Extended	0 degC	+100 degC	0 degC	+100 degC	0 degC	+100 degC
Industrial	-40 degC	+100 degC	-40 degC	+100 degC	-40 degC	+100 degC

Table 9 : Temperature Limits

Important:

If any temperature limit is exceeded, the Target FPGA is automatically cleared. This is indicated by the Green LED (Target Configured) switching off and the two status LEDs showing a temperature fault indication.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

3.8.2 Microcontroller Status LEDs

LEDs D7 (Red) and D8 (Green) indicate the microcontroller status.

LEDs	Status
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 10 : Status LED Definitions

3.9 Local Bus

A Multiplexed Packet Transport link (MPTL) connects the Bridge and Target FPGAs. It is capable of transferring data at up to 2GB/s simultaneously in each direction.

The MPTL replaces the parallel local bus used in previous generations of the ADM-XRC series. Details of the link and example designs are given in the Software Development Kit (SDK).

3.10 Target FPGA

3.10.1 Target FPGA Characteristics

The ADM-VPX3-7V2 supports Virtex-7 V585T, V2000T, VX330T, VX485T, and VX690T devices in the FF(G), FH(G), and FLG(G)1761 packages. The distinguishing characteristics of these devices are described in Table Target FPGA Characteristics. These figures are taken from the Virtex-7 FPGA Feature Summary available in the Xilinx™ 7series Overview. The maximum user I/O to the VPX backplane does not change with device selected. However FMC user I/O is reduced significanly with VX330T and VX485T devices.

Device	Logic Cells	Slices	Distributed RAM	DSP Slices	Block RAM	CMTs	PCIe Hard Macros
XC7VX330T	326,400	51,000	4,388 Kb	1,120	27,000 Kb	14	2 Gen3
XC7VX485T	485,760	75,900	8,175 Kb	2,800	37,080 Kb	14	4 Gen2
XC7VX690T	693,120	108,300	10,888 Kb	3,600	52,920 Kb	20	3 Gen3
XC7V585T	582,720	91,050	6,938 Kb	1,260	28,620 Kb	18	3 Gen2
XC7V2000T	1,954,560	305,400	21,550 Kb	2,160	46,512 Kb	24	4 Gen2

Table 11 : Target FPGA Characteristics

3.10.2 I/O Bank Voltages

The Target FPGA IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in Table Target FPGA IO Banks. Full details of the IOSTANDARD required for each signal are given in the SDK.

IO Banks	Voltage	Purpose
0, 14	1.8V	Configuration, JTAG, LBus Control, Target SelectMap Interface
13	1.8V	RGMII to 1000Base-X
39	1.8V	P2 GPIO
31, 32, 33	FMC_VADJ	FMC Interface (variable voltage, 1.8V max)
12	FMC_VIO_B	FMC Interface (variable voltage, 1.8V Max)
15, 16, 18, 19, 34, 35, 37, 38	1.5V	DRAM Banks 0-3

Table 12 : Target FPGA IO Banks

3.10.3 Target MGT Links

There are a total of 34 Multi-Gigabit Transceiver (MGT) links connected to the Target FPGA:

Links	Width	Connection
PCIe(3:0)	4	Bridge FPGA (for MPTL) or VPX P1 Wafers 1-4 in Bridge Bypass Mode
PCIe(7:4)	4	Direct link to VPX P1 Wafers 5-8
P1 Expansion(3:0)	4	Direct link to VPX P1 Wafer 9-12
User Defined(11:0)	12	Direct link to VPX P2 Wafer 7-16 and VPX P1 Wafers 13 and 14
FMC MGT(9:0)	10	Direct link to FMC interface

Table 13 : Target MGT Links

The connections of these links are shown in Figure ADM-VPX3-7V2 Block Diagram:

For MGT Clocking see Figure Clocks:

3.11 Memory Interfaces

The ADM-VPX3-7V2 has four independent banks of DDR3 SDRAM. Each bank consists of two 16 bit wide memory devices in parallel to provide a 32 bit datapath capable of running up to 800Hz (DDR-1600). 2Gb devices (Micron MT41K128M16JT-125) are fitted as standard to provide 512MB per bank. 4Gb (giving 1GB per bank) and 8Gb (2GB per bank) are available as an ordering option.

The memory banks are arranged for compatibility with the Xilinx Memory Interface Generator (MIG). Figure DRAM Banks Shows the component references and FPGA banks used. Full details of the interface, signaling standards and an example design are provided in the SDK.

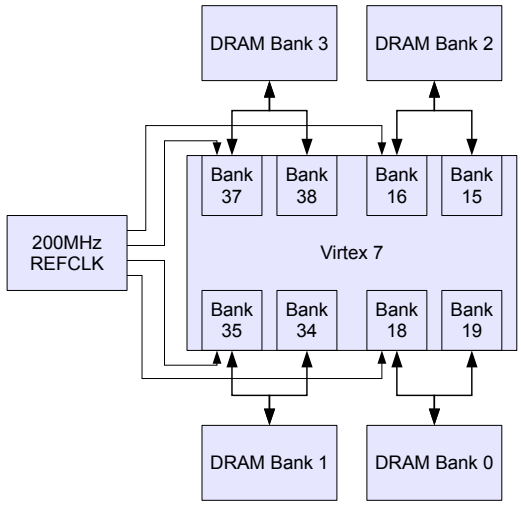

Figure 9 : DRAM Banks

Speed Grade	Single Rank (2GB-8GB)
-3	1600
-2/-2L/-2G	1600
-1	1600
-1M	1066

Table 14 : Maximum Memory Speeds

3.12 FMC Interface and Front-Panel I/O

The FMC interface provides a high-performance and flexible front-panel interface through a range of interchangeable, industry standard IO modules which connect at receptacle J3.

The FMC interface adheres to VITA 57.1. The ADM-VPX3-7V2 utilizes all possible FMC connectivity. This includes all GPIO, all MGT links, and all clock capable IO.

FMC I2C signal (SCL and SDA at C30 and C31) are connected to the system monitor microcontroller. They are used to determine operating voltage during startup and are not accesable to the user.

The FMC Present signal (PRSNT_M2C_L at connector pin H2) is buffered to FPGA pin AN33 which is a 1.8V compatible IO pin.

Note:
The ADM-VPX3-7V2 supports only 1.8V and lower VADJ Voltages.

Note:
If VX330T or VX485T FPGAs are selected as the target, the FMC interface will lose significant functionality. See pin assignments for details.

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Appendix A: P1 Pin Assignments

Appendix A.1: Data Plane (P1 Wafers 1-4)

Signal	VPX P1	FPGA	|	FPGA	VPX P1	Signal
PCIE_TX0_P or LLINK_T2B0_P	D1	J2	|	H8	A1	PCIE_RX0_P or LLINK_B2T0_P
PCIE_TX0_N or LLINK_T2B0_N	E1	J1	|	H7	B1	PCIE_RX0_N or LLINK_B2T0_N
PCIE_TX1_P or LLINK_T2B1_P	E2	H4	|	G6	B2	PCIE_RX1_P or LLINK_B2T1_P
PCIE_TX1_N or LLINK_T2B1_N	F2	H3	|	G5	C2	PCIE_RX1_N or LLINK_B2T1_N
PCIE_TX2_P or LLINK_T2B2_P	D3	G2	|	F8	A3	PCIE_RX2_P or LLINK_B2T2_P
PCIE_TX2_N or LLINK_T2B2_N	E3	G1	|	F7	B3	PCIE_RX2_N or LLINK_B2T2_N
PCIE_TX3_P or LLINK_T2B3_P	E4	F4	|	E6	B4	PCIE_RX3_P or LLINK_B2T3_P
PCIE_TX3_N or LLINK_T2B3_N	F4	F3	|	E5	C4	PCIE_RX3_N or LLINK_B2T3_N

Table 15 : Data Plane (P1 Wafers 1-4)

Note:
This bus is only connected to the target FPGA when in Bridge Bypass mode. Otherwise this bus is connected to the Alpha Data Bridge. See Table Switch Definitions for Bridge Bypass mode details.

Appendix A.2: Data/Expansion Plane (P1 Wafers 5-8)

Signal	VPX P1	FPGA	|	FPGA	VPX P1	Signal
PCIE_TX4_P	D5	K4	|	J6	A5	PCIE_RX4_P
PCIE_TX4_N	E5	K3	|	J5	B5	PCIE_RX4_N
PCIE_TX5_P	E6	L2	|	L6	B6	PCIE_RX5_P
PCIE_TX5_N	F6	L1	|	L5	C6	PCIE_RX5_N
PCIE_TX6_P	D7	M4	|	N6	A7	PCIE_RX6_P
PCIE_TX6_N	E7	M3	|	N5	B7	PCIE_RX6_N
PCIE_TX7_P	E8	N2	|	P8	B8	PCIE_RX7_P
PCIE_TX7_N	F8	N1	|	P7	C8	PCIE_RX7_N

Table 16 : Data/Expansion Plane (P1 Wafers 5-8)

Appendix A.3: Expansion/User Plane (P1 Wafers 9-14)

Signal	VPX P1	FPGA		FPGA	VPX P1	Signal
P1_TX0_P	D9	E2	|	D8	A9	P1_RX0_P
P1_TX0_N	E9	E1	|	D7	B9	P1_RX0_N
P1_TX1_P	E10	D4	|	C6	B10	P1_RX1_P
P1_TX1_N	F10	D3	|	C5	C10	P1_RX1_N
P1_TX2_P	D11	C2	|	B8	A11	P1_RX2_P
P1_TX2_N	E11	C1	|	B7	B11	P1_RX2_N
P1_TX3_P	E12	B4	|	A6	B12	P1_RX3_P
P1_TX3_N	F12	B3	|	A5	C12	P1_RX3_N
P1_TX4_P	D13	AH4	|	AE6	A13	P1_RX4_P
P1_TX4_N	E13	AH3	|	AE5	B13	P1_RX4_N
P1_TX5_P	E14	AG2	|	AD4	B14	P1_RX5_P
P1_TX5_N	F14	AG1	|	AD3	C14	P1_RX5_N

Table 17 : Expansion/User Plane (P1 Wafers 9-14)

Appendix A.4: Control Plane (P1 Wafers 15-16)

Signal	VPX P1	Component.Pin		Component.Pin	VPX P1	Signal
ETH2_TX_P	D15	U10.4	|	U10.1	A15	ETH2_RX_P
ETH2_TX_N	E15	U10.5	|	U10.2	B15	ETH2_RX_N
ETH1_TX_P	E16	U11.4	|	U11.1	B16	ETH1_RX_P
ETH1_TX_N	F16	U11.5	|	U11.2	C16	ETH1_RX_N

Table 18 : Control Plane (P1 Wafers 15-16)

The control plane 1000Base-X Ethernet on Wafer 16 is controlled by the target FPGA using an RGMII interface to a Marvell 88E1512. See pin assignment below for RGMII connectivity details.

Signal	FPGA		FPGA	Signal
ETH1_TXD0	AW36	|	AT36	ETH1_RXD0
ETH1_TXD1	AV36	|	AT34	ETH1_RXD1
ETH1_TXD2	AY34	|	AU34	ETH1_RXD2
ETH1_TXD3	BA35	|	AU36	ETH1_RXD3
ETH1_TX_CTRL	BA34	|	AT32	ETH1_RX_CTRL
ETH1_TX_CLK	AW32	|	AV34	ETH1_RX_CLK
ETH1_MDC	AU32	|	AV33	ETH1_MDIO
ETH1_CLK125	AY32	|	-	-

Table 19 : RGMII to 1000Base-X PHY

Appendix B: P2 Pin Assignments

Appendix B.1: GPIO 24s/12d + 8s (P2 Wafers 1-6)

Signal	VPX P2	FPGA		FPGA	VPX P2	Signal
GP1_P	E6	C16	|	B16	F6	GP1_N
GP2_P	B6	C15	|	C14	C6	GP2_N
GP3_P	D5	B14	|	A14	E5	GP3_N
GP4_P	A5	D16	|	D15	B5	GP4_N
GP5_P	E4	D13	|	C13	F4	GP5_N
GP6_P	B4	E12	|	D12	C4	GP6_N
GP7_P	D3	F16	|	E15	E3	GP7_N
GP8_P	A3	G12	|	F12	B3	GP8_N
GP9_P	E2	E14	|	E13	F2	GP9_N
GP10_P	B2	J13	|	H13	C2	GP10_N
GP11_P	D1	F15	|	F14	E1	GP11_N
GP12_P	A1	H16	|	G16	B1	GP12_N
GP13	G1	M13	|	N14	G3	GP14
GP15	G5	N13	|	N15	G7	GP16
GP17	G9	N16	|	M12	G11	GP18
GP19	G13	M11	|	M16	G15	GP20

Table 20 : GPIO 24s/12d + 8s (P2 Wafers 1-6)

All single ended pins can function as push-pull up to 60Mbps or Open-drain up to 2Mbps. Differential operation is limited only by FPGA IO pins. Switching between Single Ended and differential signaling is described in Table Switch Definitions.

Appendix B.2: MGT Lanes 20d (P2 Wafers 7-16)

Signal	VPX P2	FPGA		FPGA	VPX P2	Signal
P2_TX0_P	D7	U2	|	W6	A7	P2_RX0_P
P2_TX0_N	E7	U1	|	W5	B7	P2_RX0_N
P2_TX1_P	E8	T4	|	V4	B8	P2_RX1_P
P2_TX1_N	F8	T3	|	V3	C8	P2_RX1_N
P2_TX2_P	D9	R2	|	U6	A9	P2_RX2_P
P2_TX2_N	E9	R1	|	U5	B9	P2_RX2_N
P2_TX3_P	E10	P4	|	R6	B10	P2_RX3_P
P2_TX3_N	F10	P3	|	R5	C10	P2_RX3_N
P2_TX4_P	D11	AE2	|	AC6	A11	P2_RX4_P
P2_TX4_N	E11	AE1	|	AC5	B11	P2_RX4_N
P2_TX5_P	E12	AC2	|	AB4	B12	P2_RX5_P
P2_TX5_N	F12	AC1	|	AB3	C12	P2_RX5_N
P2_TX6_P	D13	AA2	|	AA6	A13	P2_RX6_P
P2_TX6_N	E13	AA1	|	AA5	B13	P2_RX6_N
P2_TX7_P	E14	W2	|	Y4	B14	P2_RX7_P
P2_TX7_N	F14	W1	|	Y3	C14	P2_RX7_N
P2_TX8_P	D15	AK4	|	AG6	A15	P2_RX8_P
P2_TX8_N	E15	AK3	|	AG5	B15	P2_RX8_N
P2_TX9_P	E16	AJ2	|	AF4	B16	P2_RX9_P
P2_TX9_N	F16	AJ1	|	AF3	C16	P2_RX9_N

Table 21 : MGT Lanes 20d (P2 Wafers 7-16)

Appendix C: FMC Pin Assignments

Appendix C.1: GPIO Pins

Signal	FMC (J1)	FPGA		FPGA	FMC (J1)	Signal
LA00_CC_P	G6	AU23	|	AV23	G7	LA00_CC_N
LA01_CC_P	D8	AT22	|	AU22	D9	LA01_CC_N
LA02_P	H7	AM24	|	AN24	H8	LA02_N
LA03_P	G9	AJ23	|	AK23	G10	LA03_N
LA04_P	H10	AK20	|	AL20	H11	LA04_N
LA05_P	D11	AL21	|	AM21	D12	LA05_N
LA06_P	C10	AJ21	|	AJ20	C11	LA06_N
LA07_P	H13	AR24	|	AT24	H14	LA07_N
LA08_P	G12	AM23	|	AN23	G13	LA08_N
LA09_P	D14	AP23	|	AP22	D15	LA09_N
LA10_P	C14	AN21	|	AP21	C15	LA10_N
LA11_P	H16	BA22	|	BB22	H17	LA11_N
LA12_P	G15	AT21	|	AU21	G16	LA12_N
LA13_P	D17	AV21	|	AW21	D18	LA13_N
LA14_P	C18	BA21	|	BB21	C19	LA14_N
LA15_P	H19	AY24	|	BA24	H20	LA15_N
LA16_P	G18	BB24	|	BB23	G19	LA16_N
LA17_CC_P	D20	AW23	|	AW22	D21	LA17_CC_N
LA18_CC_P	C22	AR23	|	AR22	C23	LA18_CC_N
LA19_P	H22	AU24	|	AV24	H23	LA19_N
LA20_P	G21	AY25	|	BA25	G22	LA20_N
LA21_P	H25	AJ22	|	AK22	H26	LA21_N
LA22_P*	G24	AU19	|	AV19	G25	LA22_N*
LA23_P*	D23	AR18	|	AR17	D24	LA23_N*
LA24_P*	H28	AN19	|	AN18	H29	LA24_N*
LA25_P*	G27	AP20	|	AR19	G28	LA25_N*
LA26_P*	D26	AV16	|	AW16	D27	LA26_N*
LA27_P*	C26	AT20	|	AT19	C27	LA27_N*
LA28_P*	H31	AK19	|	AK18	H32	LA28_N*
LA29_P*	G30	AL19	|	AM19	G31	LA29_N*
LA30_P*	H34	AK17	|	AL17	H35	LA30_N*

Table 22 : GPIO Pins **(continued on next page)**

Signal	FMC (J1)	FPGA		FPGA	FMC (J1)	Signal
LA31_P*	G33	AM18	|	AM17	G34	LA31_N*
LA32_P*	H37	AP18	|	AP17	H38	LA32_N*
LA33_P*	G36	AM16	|	AN16	G37	LA33_N*
HA00_CC_P*	F4	AV13	|	AW13	F5	HA00_CC_N*
HA01_CC_P*	E2	AU14	|	AU13	E3	HA01_CC_N*
HA02_P*	K7	AJ16	|	AJ15	K8	HA02_N*
HA03_P*	J6	AJ13	|	AJ12	J7	HA03_N*
HA04_P*	F7	AK14	|	AK13	F8	HA04_N*
HA05_P*	E6	AK15	|	AL14	E7	HA05_N*
HA06_P*	K10	AL16	|	AL15	K11	HA06_N*
HA07_P*	J9	AM12	|	AM11	J10	HA07_N*
HA08_P*	F10	AN11	|	AP11	F11	HA08_N*
HA09_P*	E9	AM13	|	AN13	E10	HA09_N*
HA10_P*	K13	AN15	|	AN14	K14	HA10_N*
HA11_P*	J12	AP12	|	AR12	J13	HA11_N*
HA12_P*	F13	AY14	|	AY13	F14	HA12_N*
HA13_P*	E12	AW12	|	AY12	E13	HA13_N*
HA14_P*	J15	BB14	|	BB13	J16	HA14_N*
HA15_P*	F16	BA15	|	BA14	F17	HA15_N*
HA16_P*	E15	AV15	|	AV14	E16	HA16_N*
HA17_CC_P*	K16	AP13	|	AR13	K17	HA17_CC_N*
HA18_P*	J18	BA16	|	BB16	J19	HA18_N*
HA19_P*	F19	AR15	|	AT15	F20	HA19_N*
HA20_P*	E18	AR14	|	AT14	E19	HA20_N*
HA21_P*	K19	AT12	|	AU12	K20	HA21_N*
HA22_P*	J21	AY19	|	BA19	J22	HA22_N*
HA23_P*	K22	AY20	|	BA20	K23	HA23_N*
HB00_CC_P*	K25	AR27	|	AT27	K26	HB00CC__N*
HB01_P*	J24	BA26	|	BA27	J25	HB01_N*
HB02_P*	F22	AV25	|	AV26	F23	HB02_N*
HB03_P*	E21	BB26	|	BB27	E22	HB03_N*
HB04_P*	F25	AY27	|	AY28	F26	HB04_N*
HB05_P*	E24	BB28	|	BB29	E25	HB05_N*
HB06_CC_P*	K28	AU26	|	AU27	K29	HB06_CC_N*
HB07_P*	J27	AW27	|	AW28	J28	HB07_N*
HB08_P*	F28	AU29	|	AV29	F29	HB08_N*

Table 22 : GPIO Pins (continued on next page)

Signal	FMC (J1)	FPGA		FPGA	FMC (J1)	Signal
HB09_P*	E27	AW25	|	AW26	E28	HB09_N*
HB10_P*	K31	AR29	|	AT29	K32	HB10_N*
HB11_P*	J30	AU28	|	AV28	J31	HB11_N*
HB12_P*	F31	AN28	|	AP28	F32	HB12_N*
HB13_P*	E30	AT25	|	AT26	E31	HB13_N*
HB14_P*	K34	AL25	|	AL26	K35	HB14_N*
HB15_P*	J33	AM26	|	AM27	J34	HB15_N*
HB16_P*	F34	AK27	|	AL27	F35	HB16_N*
HB17_CC_P*	K37	AP27	|	AR28	K38	HB17_CC_N*
HB18_P*	J36	AK24	|	AK25	J37	HB18_N*
HB19_P*	E33	AP25	|	AR25	E34	HB19_N*
HB20_P*	F37	AN25	|	AN26	F38	HB20_N*
HB21_P*	E36	AJ25	|	AJ26	E37	HB21_N*
FMC_CLK_DIR_-1V8*	B1	BB12	|	-	-	-

Table 22 : GPIO Pins

Appendix C.2: Clock Pins

Signal	FMC (J1)	FPGA		FPGA	FMC (J1)	Signal
GBTCLK0_M2C_P*	D4	AT8	|	AT7	D5	GBTCLK0_M2C_N*
GBTCLK1_M2C_P*	B20	AU10	|	AU9	B21	GBTCLK1_M2C_N*
CLK0_M2C_P*	H4	AY18	|	AY17	H5	CLK0_M2C_N*
CLK1_M2C_P*	G2	AT17	|	AU17	G3	CLK1_M2C_N*
CLK2_BIDIR_P*	K4	AU18	|	AV18	K5	CLK2_BIDIR_N*
CLK3_BIDIR_P*	J2	AW18	|	AW17	J3	CLK3_BIDIR_N*

Table 23 : Clock Pins

* For XCVX330T or XCVX485T pins not connected

Appendix C.3: MGT Pins

Signal	FMC (J1)	FPGA		FPGA	FMC (J1)	Signal
DP0_M2C_P	C6	AN6	|	AP4	C2	DP0_C2M_P
DP0_M2C_N	C7	AN5	|	AP3	C3	DP0_C2M_N
DP1_M2C_P	A2	AM8	|	AN2	A22	DP1_C2M_P
DP1_M2C_N	A3	AM7	|	AN1	A23	DP1_C2M_N
DP2_M2C_P	A6	AL6	|	AM4	A26	DP2_C2M_P
DP2_M2C_N	A7	AL5	|	AM3	A27	DP2_C2M_N
DP3_M2C_P	A10	AJ6	|	AL2	A30	DP3_C2M_P
DP3_M2C_N	A11	AJ5	|	AL1	A31	DP3_C2M_N
DP4_M2C_P*	A14	AV8	|	AV4	A34	DP4_C2M_P*
DP4_M2C_N*	A15	AV7	|	AV3	A35	DP4_C2M_N*
DP5_M2C_P*	A18	AU6	|	AU2	A38	DP5_C2M_P*
DP5_M2C_N*	A19	AU5	|	AU1	A39	DP5_C2M_N*
DP6_M2C_P*	B16	AR6	|	AT4	B36	DP6_C2M_P*
DP6_M2C_N*	B17	AR5	|	AT3	B37	DP6_C2M_N*
DP7_M2C_P*	B12	AP8	|	AR2	B32	DP7_C2M_P*
DP7_M2C_N*	B13	AP7	|	AR1	B33	DP7_C2M_N*
DP8_M2C_P*	B8	BB8	|	BB4	B28	DP8_C2M_P*
DP8_M2C_N*	B9	BB7	|	BB3	B29	DP8_C2M_N*
DP9_M2C_P*	B4	BA6	|	BA2	B24	DP9_C2M_P*
DP9_M2C_N*	B5	BA5	|	BA1	B25	DP9_C2M_N*

Table 24 : MGT Pins

* For XCVX330T or XCVX485T pins not connected

Revision History

Date	Revision	Changed By	Nature of Change
10 Oct 2012	0.1	K. Roth	Initial Draft
14 Mar 2013	1.0	K. Roth	Initial Release , finalized appendix
29 Oct 2013	1.1	K. Roth	Updated Figure Clocks to 25MHz onboard oscilator, Table PROGCLK Connections fixed to show PROGCLK [4:0] instead of[3:0], Updated miscellaneous Appendix table column headers to show VPX P1 where appropriate.
14 Nov 2013	1.2	K. Roth	Updated Section AUXCLK to show pin assignments.
19 Nov 2013	1.3	K. Roth	Updated Figure ADM-VPX3-7V2 Block Diagram and Table RGMII to 1000Base-X PHY.
23 Jan 2014	1.4	K. Roth	Added Section VPX P2 GPIO
6 Feb 2014	1.5	K. Roth	Corrected PROGCLK0 and PROGCLK1 in Clocks
18 Feb 2014	1.6	K. Roth	Changed System Requirements to specify 5.0 V as the default VPWR option.
8 Jul 2014	1.7	K. Roth	Added Automatic Temperature Monitoring and Maximum Memory Speeds
16 Oct 2015	1.8	K. Roth	Updated JTAG Interface to correct J3 reference designation, FMC Interface and Front-Panel I/O to include FMC Present and I2C description, and added 25MHz Source.
22 Aug 2016	1.9	K. Roth	Updated Memory Interfaces to remove dual rank 8Gb option as micron has moved this part to single rank.

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